

Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS₂

Vinod K. Sangwan¹, Deep Jariwala¹, In Soo Kim¹, Kan-Sheng Chen¹, Tobin J. Marks^{1,2}, Lincoln J. Lauhon^{1*} and Mark C. Hersam^{1,2*}

Continued progress in high-speed computing depends on breakthroughs in both materials synthesis and device architectures^{1–4}. The performance of logic and memory can be enhanced significantly by introducing a memristor^{5,6}, a two-terminal device with internal resistance that depends on the history of the external bias voltage^{5–7}. State-of-the-art memristors, based on metal-insulator-metal (MIM) structures with insulating oxides, such as TiO₂, are limited by a lack of control over the filament formation and external control of the switching voltage^{3,4,6,8,9}. Here, we report a class of memristors based on grain boundaries (GBs) in single-layer MoS₂ devices^{10–12}. Specifically, the resistance of GBs emerging from contacts can be easily and repeatedly modulated, with switching ratios up to $\sim 10^3$ and a dynamic negative differential resistance (NDR). Furthermore, the atomically thin nature of MoS₂ enables tuning of the set voltage by a third gate terminal in a field-effect geometry, which provides new functionality that is not observed in other known memristive devices.

In this work, memristors were fabricated from monolayer MoS₂ films grown on oxidized Si substrates (300 nm SiO₂) by chemical vapour deposition (CVD) sulphurization of MoO₃ films (see Methods and Supplementary Section 1). Two Au electrodes on the MoS₂ define the memristor channel and an additional gate electrode (Si) is used to control the set voltage (Fig. 1a). The best-performing devices have GBs that are connected to only one of the two electrodes (Fig. 1a and Supplementary Fig. 2). We refer to such devices as intersecting-GB memristors. As-fabricated devices were preconditioned to a switchable state by an electroforming process that causes irreversible changes in the current–voltage (*I*–*V*) characteristics (Supplementary Sections 2 and 3). Electroformed intersecting-GB memristors show a high-resistance state (HRS) at *V* = 0 V that changes to a low-resistance state (LRS) at a high bias after an abrupt increase in current (Fig. 1b, set process, sweep i). The device stays in the LRS as the voltage is decreased to zero (sweep ii). The ratio of resistance in the bistable states at zero bias, $R_{\text{HRS}}/R_{\text{LRS}}$, is $\sim 10^3$ (Fig. 1c, inset). In the negative bias sweep, the device begins in the LRS (sweep iii) and then changes to the HRS (reset process, sweep iv). The pinched hysteresis loop in *I*–*V* with *I* = 0 at *V* = 0 indicates the presence of a memristive element within the device^{5–7}. Furthermore, the device shows a sudden increase in current (conductance $G \equiv \partial I / \partial V = 175 \mu\text{S}$) within a single bias step of 0.1 V (Fig. 1b). This current spike is followed by a dynamic NDR that is commonly observed in memristive systems^{4,13}. This dynamic NDR depends on the sweep rate and is therefore different from the static NDR observed in resonant devices^{4,6}. Sweep i is described by $I \propto V^m$ (*V* < 8.5 V, Fig. 1c), where *m* increases monotonically with bias. This type of dependence is characteristic of space-charge-limited current, which has

been observed in complex-oxide memristors¹⁴ as well as in monolayer MoS₂ transistors^{15,16}. The present MoS₂ memristors show 100× smaller set fields ($\sim 10^4 \text{ V cm}^{-1}$ for $V_{\text{set}} = 8.3 \text{ V}$ in Fig. 1b) than those in conventional memristors, and thereby promise switches and memories of low dynamic power (the standard operating point of *V* = *I* = 0 makes the static power of memristors inherently low).

Devices with different GB orientations were analysed to identify the switching mechanism. The bridge-GB memristor contains a GB parallel to the channel and bridging the two electrodes (Fig. 1d,e). After electroforming (Supplementary Section 2), the bridge-GB memristor *I*–*V* shows an extremely rapid current increase (*G* > 1 mS, Fig. 1d,e) followed by an NDR that is larger than that observed in intersecting-GB memristors (Fig. 1b). In contrast to intersecting-GB memristors, bridge-GB memristors do not exhibit bistable states of different resistances at *V* = 0 V. Furthermore, the gate voltage (*V_g*)-modulated current ratio decreases dramatically from $\sim 5 \times 10^4$ in the pristine state to ~ 2 in the electroformed state (Supplementary Fig. 6c), which suggests the formation of a highly conducting filament between the electrodes. In contrast, the bisecting-GB memristor features a GB perpendicular to the channel that does not contact either of the electrodes and possesses a bipolar resistive switching that shows a broad current peak followed by a slow current decay in the NDR regime with $R_{\text{HRS}}/R_{\text{LRS}} \approx 4$ at zero bias (Fig. 1f,g and Supplementary Section 4).

The dependencies of these memristive phenomena on the GB geometry, together with the absence of memristive behaviour in the control devices without GBs (Supplementary Section 5) and repeatable multiple sweeps (Supplementary Section 6), suggest the following mechanism for the conductance modulation in intersecting-GB memristors. The electroforming process increases the overall resistance of the device in the off state by removing mobile dopants (identified below) from the region between the GB tip and the opposing electrode. During the set process, dopants migrate from the GB region to the depleted region, and thus increase the conductance (on). The dopants are driven away from the drain electrode and towards the GB region during the reset process, turning the device off. The power law *I*–*V* characteristics (as opposed to exponential *I*–*V*), two-terminal versus four-terminal measurements (Supplementary Sections S2) and comparisons between the Au and Ti contacts (Supplementary Section 3) rule out a Schottky barrier formation near the contacts via anion segregation, as seen in TiO₂ memristors⁹. Direct evidence of GB migration was found in a device that contained both a bisecting-GB and a GB connected to one of the electrodes (Fig. 2). After multiple sweeps at high biases ($\pm 40 \text{ V}$), the bisecting GB shifted by up to 3 μm . A similar significant motion of extended defects in two-dimensional materials has been observed in atomic-scale

¹Department of Materials Science and Engineering, Northwestern University, Evanston, Illinois 60208, USA. ²Department of Chemistry, Northwestern University, Evanston, Illinois 60208, USA. *e-mail: lauho@northwestern.edu; m-hersam@northwestern.edu

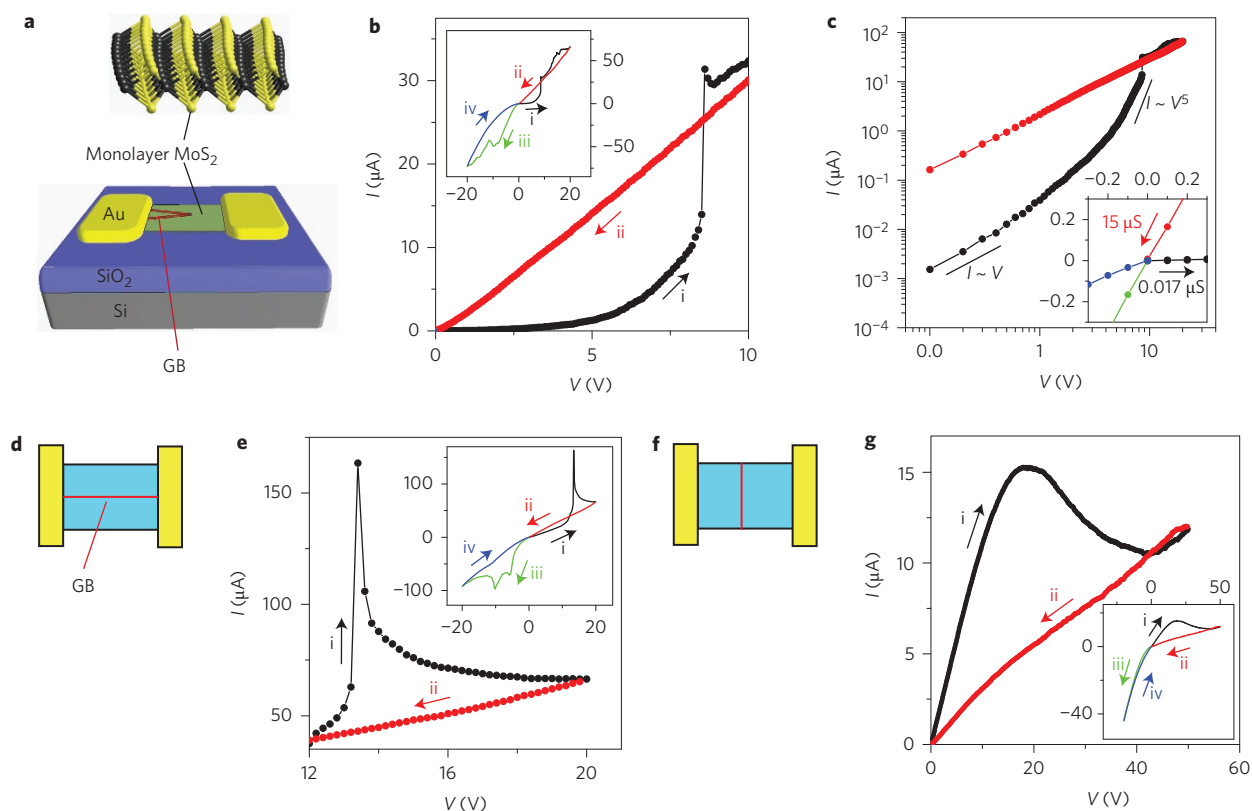


Figure 1 | *I*-*V* characteristics of MoS₂ memristors. **a**, Schematic of an intersecting-GB MoS₂ memristor with two GBs connected to one of the electrodes and intersecting at a vertex within the channel. **b**, Partial *I*-*V* characteristics of an electroformed intersecting-GB memristor (channel length, $L = 7 \mu\text{m}$; see Supplementary Section 1 for AFM images) obtained immediately after the electroforming process described in Supplementary Section 2. The set process occurs at $V_{\text{set}} = 8.3 \text{ V}$ with an abrupt twofold increase in current. Inset: Full *I*-*V* characteristics of one switching cycle. Measurements were performed at a sweep rate of 1 V s^{-1} and $V_g = 40 \text{ V}$ under vacuum (pressure $< 2 \times 10^{-5}$ torr). The voltage was swept in the order $0 \text{ V} \rightarrow 20 \text{ V} \rightarrow 0 \text{ V} \rightarrow -20 \text{ V} \rightarrow 0 \text{ V}$, as shown by the coloured arrows with the four sweeps labelled as i, ii, iii and iv. **c**, Log-log plot of sweeps i and ii from **b**, which shows space-charge limited and ohmic transport in sweeps i and ii, respectively. Sweep i also shows an ohmic *I*-*V* behaviour at a low bias ($V < 0.5 \text{ V}$). The inset shows a zoomed-in *I*-*V* curve from the inset of **b** near a zero bias, which reveals conductance values $G (\equiv dI/dV)$ in the off (HRS) and on (LRS) states. **d,e**, A schematic (**d**) and partial *I*-*V* characteristic (**e**) of an electroformed bridge-GB memristor ($L = 7.5 \mu\text{m}$; see Fig. 3f and Supplementary Section 8 for AFM images) at $V_g = 40 \text{ V}$ showing a transient current spike ($V_{\text{set}} = 13.2 \text{ V}$) followed by an NDR regime. The inset shows the full *I*-*V* characteristics of one switching cycle. The voltage sweeps were conducted in the order i, ii, iii, iv, as indicated by the coloured arrows (sweep rate = 2 V s^{-1}). **f,g**, A schematic (**f**) and partial *I*-*V* characteristic (**g**) of an electroformed bisecting-GB memristor (see Supplementary Section 1 for an optical image and Supplementary Section 2 for the electroforming process) at $V_g = 55 \text{ V}$ showing a broad current peak followed by an NDR regime. The inset shows full *I*-*V* characteristics of one switching cycle. Bias sweeps were conducted in the order i, ii, iii, iv, as indicated by the coloured arrows (sweep rate = 2 V s^{-1}).

transmission electron microscopy images of migrating dislocations in CVD-grown single-layer WS₂ (ref. 16).

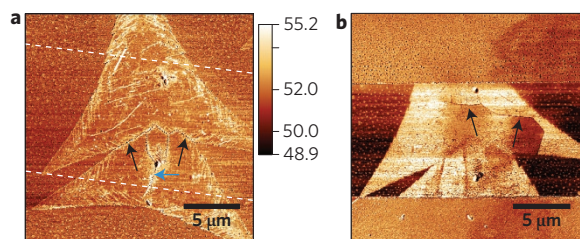


Figure 2 | GB migration. **a**, AFM phase image of an MoS₂ flake with multiple GBs. The dashed white lines indicate the location of the electrode edges after device fabrication in **b**. One GB (highlighted by black arrows) bisects the channel and another GB (blue arrow) touches the lower electrode edge. **b**, AFM phase image of the device after a series of 12 sweep cycles in the range 40 V to -40 V (sweep rate = 1 V s^{-1}). Black arrows in **a,b**, show that the GBs have migrated by up to $3 \mu\text{m}$. Colour scale bars show the phase angles in degrees.

Electrostatic force microscopy (EFM) and spatially resolved photoluminescence (PL) spectroscopy are used to elucidate further the switching mechanism in the present devices (Fig. 3). In contrast to buried MIM memristors, all-surface monolayer MoS₂ memristors provide a new platform for the *in situ* probing of the underlying mechanisms in nanoionic switches. The abrupt change of the cantilever phase in the EFM images of Fig. 3c–e (and Supplementary Section 7) across a bisecting GB (see Methods) indicates that the electrostatic potential drops primarily at the GB (that is, the GB is resistive). This conclusion is consistent with the overall higher resistance of the bisecting-GB memristor compared to the bridge-GB memristor. However, sulphur vacancies in MoS₂ have been shown to accumulate near GBs^{11,17}, and both the midgap states of sulphur vacancies^{11,18} and the electrons donated by dangling bonds should render the MoS₂ regions near GBs more conductive. Therefore, we expect that the resistance of devices with GBs can be modulated to the extent that the sulphur vacancy concentrations in adjacent regions are modulated by vacancy migration. It follows that an electric field applied parallel to an intersecting GB will promote migration of vacancies between the GB and the depletion region. Circumstantial evidence of the key role of

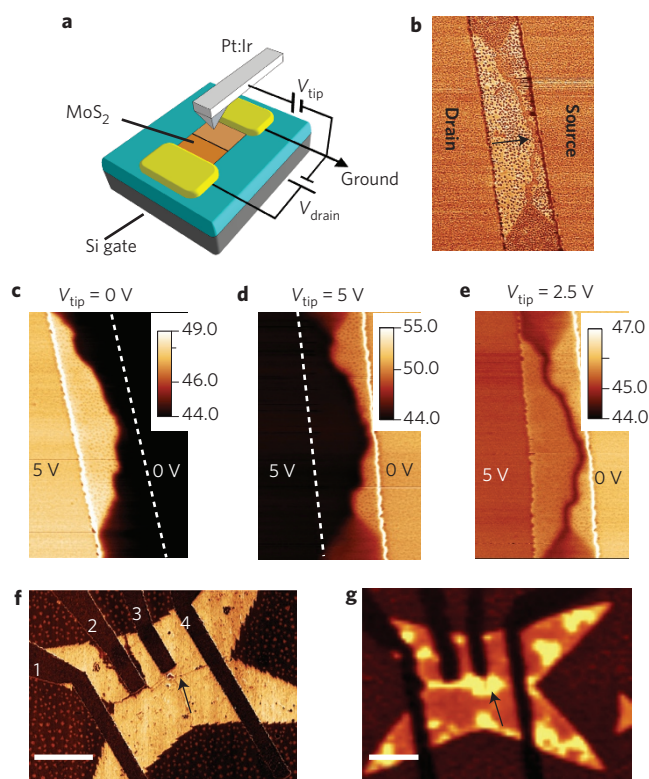


Figure 3 | EFM and spatially resolved PL images. **a**, A schematic of the EFM measurement of the channel of a biased bisecting-GB memristor under an inert environment (see Methods). Bias voltages of the tip and drain electrode are varied while the source electrode and back gate Si are grounded. **b**, AFM phase image of an electroformed bisecting-GB device shows a GB (highlighted by a black arrow) that divides the channel into two regions connected to drain and source electrodes, respectively. The channel length of the device is 2 μm . **c–e**, Corresponding EFM phase images of the device from **b** at tip biases $V_{\text{tip}} = 5 \text{ V}$, 0 V and 2.5 V , respectively. Colour scale bars show the EFM phase in degrees. Device bias conditions: $V_{\text{drain}} = 5 \text{ V}$ and $V_{\text{source}} = V_{\text{g}} = 0 \text{ V}$. The dotted lines highlight the metal-MoS₂ junctions with less contrast. **f**, AFM phase image of an electroformed bridge-GB memristor with a GB that connects both of the electrodes (highlighted by a black arrow). Only electrodes 1 and 4 of the van der Pauw geometry were used for electrical measurement, with electrodes 2 and 3 kept floating (Supplementary Section 2). **g**, Spatial mapping of the area under the PL excitonic peaks A and B (see Supplementary Section 8) of the MoS₂ device in **f** that shows an increased PL intensity in the GB (black arrow). Scale bars (**f**, **g**), 4 μm . See Supplementary Section 8 for correlated PL and Raman mapping and analyses.

sulphur vacancies is provided by the fact that these memristive phenomena are observed only in devices that are intentionally grown to produce sulphur vacancies, according to methods we recently reported¹⁹.

PL and Raman spectroscopy maps of electroformed devices provide additional evidence for higher concentrations of sulphur vacancies near GBs (Fig. 3f,g and Supplementary Section 8). First, PL emission is enhanced near the GBs in the bridge-GB and intersecting-GB memristors (Fig. 3f,g and Supplementary Section 8), as was also reported previously¹¹, and it is associated with sulphur vacancies. In addition, the PL blue-shift and Raman blue-shift are consistent with O₂ chemisorption at sulphur vacancies²⁰ (Supplementary Section 8). Thus, spatially resolved analyses confirm that an increased density of defects exists near GBs following electroforming. Sulphur vacancies are the most-probable candidates for mobile anionic species within MoS₂. Mobile Mo cations

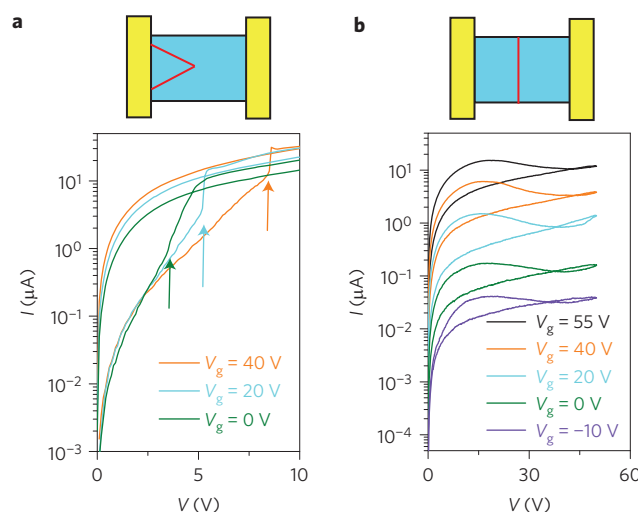


Figure 4 | Gate-tunability of an intersecting-GB and a bisecting-GB memristor. **a**, Log-linear plot that shows the I - V characteristics of an intersecting-GB memristor at different V_{g} . The full V sweep range is 20 to -20 V . Switching the set voltage (shown by coloured arrows at $V_{\text{set}} = 3.5, 5$ and 8 V) is controlled by V_{g} . **b**, Log-linear plot of I - V characteristics ($V > 0 \text{ V}$) of a bisecting-GB memristor at different V_{g} . The full V sweep range is 50 to -20 V . The negative bias sweep range is limited to -20 V to avoid a dielectric breakdown between the gate and the drain electrode. The current in both the LRS and HRS is modulated by three orders of magnitude by V_{g} .

are unlikely to be relevant because of the absence of an electrolytic medium or an electrochemically active metal⁴.

The proposed migration mechanism of mobile anions can also account for the switching characteristics in bridge-GB and bisecting-GB memristors. In bridge-GB memristors, anions segregate near the GB during electroforming, which increases the conductivity of the boundary, similar to vacancy migration in ZnO²¹, TiO₂^{6,9} and TaO_x memristors²². The switching in Fig. 1e proceeds through a two-step process: first, the region near the GB becomes highly conducting at a high bias because of the metallic-like transport across interacting defects at a high density^{23,24}; second, Joule heating leads to a thermal rupture of the filament, which induces an NDR similar to that of threshold switching^{4,13,25}. Thus, volatile switching and the NDR regime result from the decreasing width of the defect-rich region via the lateral drift of anions⁴. The absence of bistable states at $V = 0 \text{ V}$ in bridge-GB memristors is akin to complementary resistive switching in TaO_x memristors²⁶. In contrast, the broad current peak, NDR features and asymmetric I - V characteristics²⁷ of bisecting-GB memristors are reminiscent of soft switching in non-filamentary GaO_x memristors²⁸ and Cr-doped SrZrO₃ memristors²⁷. The hysteretic I - V (Fig. 1g) can be explained by the dynamic and nonlinear relation between drift (driven by electric field) and diffusion (driven by the concentration gradient) of anions to form depletion regions on either side of the bisecting GB^{6,7}.

Finally, we show that the present three-terminal MoS₂ memristors are gate tunable, which has not been observed in previous memristive systems and thus presents new opportunities for memristive circuits and related applications. In intersecting-GB memristors, the set voltage (V_{set}) can be varied from 3.5 to 8.0 V by varying the gate bias from 0 to 40 V (Fig. 4a), which suggests that independently addressable local gates in MoS₂ memristors could continuously adjust V_{set} to afford fault-tolerant architectures²⁹. Furthermore, a controlled V_{set} allows additional flexibility in designing complementary and bipolar resistive switching^{1,8,30}. Bisecting-GB memristors offer an additional gate-tunable functionality, namely that the

resistance values in each of the bistable states at zero bias can be controlled by more than three orders of magnitude (Fig. 4b), whereas the switching ratio (~ 4 – 6) and shape of the set curves remain relatively unchanged with V_g . This adjustable resistance could be used as continuous-weight synapses in neuromorphic circuits^{29,31}. Independent control of device resistances can also lead to better uniformity and impedance matching between memristive circuits. Gate-tunable memristors further present opportunities for hybrid complementary metal–oxide semiconductor memristor field-programmable architectures^{29,32}.

Methods

Devices fabrication and measurement. Monolayer MoS₂ flakes were grown by CVD^{11,17,19}. The extent of sulphurization was controlled by heating the sulphur vapour to 150 °C and by restricting the time of exposure to sulphur vapour to three minutes. A higher sulphur vapour temperature (~ 170 °C) and a longer duration of exposure (ten minutes) results in stoichiometric triangular flakes¹⁹. As calculated from the shift in the threshold voltage, MoS₂ flakes grown at a reduced sulphur vapour pressure show a defect-induced doping level of approximately $\sim 1.7 \times 10^{12} \text{ cm}^{-2}$. A quantitative estimation of the stoichiometry at different growth conditions is reported in Kim *et al.*¹⁹. Atomic force microscopy (AFM) and Raman spectroscopy were used to identify the monolayer MoS₂ and GBs (Supplementary Section 1). The devices were fabricated using electron-beam lithography, as in a previously reported procedure³³. The electrodes (70 nm Au and 2 nm Ti) were deposited by thermal evaporation. After the lift-off process, the devices were submerged in *N*-methyl-2-pyrrolidone at 80 °C for 30 minutes to remove processing residues. All electroforming processes and electrical measurements were performed under vacuum (pressure $< 2 \times 10^{-5}$ torr) using a LakeShore CRX 4 K probe station and Keithley 2400 source-meters.

Scanning probe microscopy. AFM and EFM scans were performed in an Asylum Cypher ES system. All the AFM images were taken in the tapping mode using NCHR tips (NanoWorld Inc.). The resonance frequency of these cantilevers is ~ 300 kHz, and the nominal diameter of the tip apex is ~ 10 nm. The tapping mode imaging is operated in the repulsive regime by maintaining the phase signal below 90° throughout the entire scan. For EFM imaging, the cantilever amplitude was set to the same value as that of the tapping mode imaging while maintaining a distance of ~ 50 nm from the surface to avoid damage to the tip from tall electrodes (70 nm). EFM tips (NanoWorld Pointprobe EFM) were monolithic Si coated with PtIr. The typical tip radius and resonant frequency were 25 nm and 75 kHz, respectively. EFM scans were captured on wire-bonded devices placed inside an inert environment cell that consisted of continuously flowing pure nitrogen. Device electrical biasing was achieved during the EFM by using Keithley source meters.

PL spectroscopy. Micro-PL measurements were conducted using a confocal Raman system (WITec Alpha 300R) equipped with a 532 nm excitation source. The laser was focused using a $\times 100$ objective (numerical aperture 0.9), and the power was kept below ~ 50 μW to avoid laser-induced sample heating and/or damage. As the spatial resolution of the system is ~ 350 nm, a 300 nm step size was used for the PL mapping. A 600 g mm⁻¹ grating dispersed the photons prior to collection by a Si-based CCD (charge-coupled device) camera.

Received 19 August 2014; accepted 23 February 2015;
published online 6 April 2015

References

- Linn, E., Rosezin, R., Kügler, C. & Waser, R. Complementary resistive switches for passive nanocrossbar memories. *Nature Mater.* **9**, 403–406 (2010).
- Theis, T. N. & Solomon, P. M. In quest of the next switch: prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor. *Proc. IEEE* **98**, 2005–2014 (2010).
- Waser, R. & Aono, M. Nanoionics-based resistive switching memories. *Nature Mater.* **6**, 833–840 (2007).
- Yang, J. J., Strukov, D. B. & Stewart, D. R. Memristive devices for computing. *Nature Nanotech.* **8**, 13–24 (2013).
- Chua, L. Memristor—the missing circuit element. *IEEE Trans. Circuit Theory* **18**, 507–519 (1971).
- Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. *Nature* **453**, 80–83 (2008).
- Chua, L. Resistance switching memories are memristors. *Appl. Phys. A* **102**, 765–783 (2011).
- Borghetti, J. *et al.* ‘Memristive’ switches enable ‘stateful’ logic operations via material implication. *Nature* **464**, 873–876 (2010).
- Yang, J. J. *et al.* Memristive switching mechanism for metal/oxide/metal nanodevices. *Nature Nanotech.* **3**, 429–433 (2008).

- Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J. & Hersam, M. C. Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. *ACS Nano* **8**, 1102–1120 (2014).
- van der Zande, A. M. *et al.* Grains and grain boundaries in highly crystalline monolayer molybdenum disulphide. *Nature Mater.* **12**, 554–561 (2013).
- Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS₂ transistors. *Nature Nanotech.* **6**, 147–150 (2011).
- Pickett, M. D., Borghetti, J., Yang, J. J., Medeiros-Ribeiro, G. & Williams, R. S. Coexistence of memristance and negative differential resistance in a nanoscale metal–oxide–metal system. *Adv. Mater.* **23**, 1730–1733 (2011).
- Xia, Y., He, W., Chen, L., Meng, X. & Liu, Z. Field-induced resistive switching based on space-charge-limited current. *Appl. Phys. Lett.* **90**, 022907 (2007).
- Ghatak, S. & Ghosh, A. Observation of trap-assisted space charge limited conductivity in short channel MoS₂ transistor. *Appl. Phys. Lett.* **103**, 122103 (2013).
- Azizi, A. *et al.* Dislocation motion and grain boundary migration in two-dimensional tungsten disulphide. *Nature Commun.* **5**, 4867 (2014).
- Najmaei, S. *et al.* Vapour phase growth and grain boundary structure of molybdenum disulphide atomic layers. *Nature Mater.* **12**, 754–759 (2013).
- Chen, M. *et al.* Multibit data storage states formed in plasma-treated MoS₂ transistors. *ACS Nano* **8**, 4023–4032 (2014).
- Kim, I. S. *et al.* Influence of stoichiometry on the optical and electrical properties of chemical vapor deposition derived MoS₂. *ACS Nano* **8**, 10551–10558 (2014).
- Nan, H. *et al.* Strong photoluminescence enhancement of MoS₂ through defect engineering and oxygen bonding. *ACS Nano* **8**, 5738–5745 (2014).
- Shen, X., Puzyrev, Y. S. & Pantelides, S. T. Vacancy breathing by grain boundaries—a mechanism of memristive switching in polycrystalline oxides. *MRS Commun.* **3**, 167–170 (2013).
- Kim, S., Choi, S. & Lu, W. Comprehensive physical model of dynamic resistive switching in an oxide memristor. *ACS Nano* **8**, 2369–2376 (2014).
- Jariwala, D. *et al.* Band-like transport in high mobility unencapsulated single-layer MoS₂ transistors. *Appl. Phys. Lett.* **102**, 173107 (2013).
- Najmaei, S. *et al.* Electrical transport properties of polycrystalline monolayer molybdenum disulfide. *ACS Nano* **8**, 7930–7937 (2014).
- Chang, S. *et al.* Occurrence of both unipolar memory and threshold resistance switching in a NiO film. *Phys. Rev. Lett.* **102**, 026801 (2009).
- Yang, Y., Sheridan, P. & Lu, W. Complementary resistive switching in tantalum oxide-based resistive memory devices. *Appl. Phys. Lett.* **100**, 203112 (2012).
- Park, J.-W. *et al.* Resistive switching characteristics and set-voltage dependence of low-resistance state in sputter-deposited SrZrO₃/Cr memory films. *J. Appl. Phys.* **99**, 124102 (2006).
- Aoki, Y. *et al.* Bulk mixed ion electron conduction in amorphous gallium oxide causes memristive behaviour. *Nature Commun.* **5**, 3473 (2014).
- Likharev, K. K. Hybrid CMOS/nanoelectronic circuits: opportunities and challenges. *J. Nanoelectron. Optoelectron.* **3**, 203–230 (2008).
- Linn, E., Rosezin, R., Tappertzhofen, S., Böttger, U. & Waser, R. Beyond von Neumann—logic operations in passive crossbar arrays alongside memory operations. *Nanotechnology* **23**, 305205 (2012).
- Snider, G. S. Self-organized computation with unreliable, memristive nanodevices. *Nanotechnology* **18**, 365202 (2007).
- Xia, Q. *et al.* Memristor–CMOS hybrid integrated circuits for reconfigurable logic. *Nano Lett.* **9**, 3640–3645 (2009).
- Sangwan, V. K. *et al.* Low-frequency electronic noise in single-layer MoS₂ transistors. *Nano Lett.* **13**, 4351–4355 (2013).

Acknowledgements

This research was supported by the Materials Research Science and Engineering Center (MRSEC) of Northwestern University (NSF DMR-1121262) and the Office of Naval Research (N00014-14-1-0669). This work made use of the Electron Probe Instrumentation Center facility (Northwestern University Atomic and Nanoscale Characterization Experimental Center, Northwestern University), which has received support from the MRSEC (NSF DMR-1121262), Nanoscale Science and Engineering Center (NSF EEC-0118025/003), State of Illinois and Northwestern University.

Author contributions

V.K.S., T.J.M., L.J.L. and M.C.H. designed the experiments. V.K.S. and D.J. fabricated and measured the devices. I.S.K. performed the CVD, photoluminescence and Raman microscopy. V.K.S. and K.-S.C. conducted the scanning probe microscopy (AFM/EFM) measurements. All authors wrote the manuscript and discussed the results at all stages.

Additional information

Supplementary information is available in the [online version](#) of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to L.J.L. and M.C.H.

Competing financial interests

The authors declare no competing financial interests.